Commerce CHIPS Act Programs: Status Report

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This report provides the status of programs under the CHIPS Act of 2022 that are administered by the Department of Commerce's National Institute of Standards and Technology (NIST). This status report describes the actions taken by the CHIPS Program Office (CPO) and the CHIPS Research and Development Office (CRDO), which are the two NIST offices responsible for implementing the semiconductor incentive programs and research and development initiatives, respectively. This report covers the period August 9, 2022, to January 31, 2025.

On March 31, 2025, the President issued an executive order establishing the United States Investment Accelerator[1] within the Department of Commerce. This new office assumed responsibility for CPO and is intended to facilitate and accelerate investments above $1 billion.

Commerce OIG is responsible for oversight of the implementation and management of CHIPS Act programs. This report follows the Council of Inspectors General on Integrity and Efficiency's *Quality Standards for Inspection and Evaluation* and provides a status update without making recommendations.

CHIPS Status At A Glance

CPO has made 20 awards for up to $33.7 billion in direct funding and up to $5.5 billion in loans.

CRDO has awarded almost $8.3 billion to operate the National Semiconductor Technology Center and to fund research projects to bring new CHIPS technology to the commercial market.

Why This Matters

According to the Congressional Research Service, the United States has seen a decline in its leadership in semiconductor chip manufacturing and research over recent decades. To counter this and strengthen domestic semiconductor production and innovation, Congress passed the Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act in August 2022.

A division of the CHIPS and Science Act, the CHIPS Act provides $50 billion to the Department of Commerce to support semiconductor research, development, innovation, and manufacturing, along with authorization for up to $75 billion in direct loans and loan guarantees.

For further details on OIG's CHIPS oversight efforts, see p. 19.

[1] The Investment Accelerator will assist investors as they navigate regulatory processes, reduce regulatory burdens and increase access to and use of national resources where consistent with applicable law, facilitate research collaborations with national labs, and work with state governments in all 50 states to reduce regulatory barriers to and increase domestic and foreign investment in the United States.

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About the CHIPS Act

The CHIPS Act of 2022 (division A of the CHIPS and Science Act)* authorizes direct funding (including grants, cooperative agreements, and other transactions) to support research and development, innovation, and manufacturing related to semiconductors.† This includes investments in manufacturing facilities, workforce development, and collaborations between government agencies and private companies.

The CHIPS Act provides $50 billion to the Department of Commerce, with $39 billion dedicated to direct funding for incentivizing investment in facilities and equipment for the fabrication, assembly, testing, advanced packaging, or research and development of domestic semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment, and $11 billion designated for establishing a robust domestic semiconductor research and development ecosystem. In addition, the CHIPS Act provides for up to $75 billion in loan authority.

* Pub. L No. 117-167, 136 Stat. 1366 (2022).

† The CHIPS Act of 2022 amended Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021; we refer to these provisions collectively as the CHIPS Act.

CHIPS Program Office

Overview

Of the $50 billion provided to the Department by the CHIPS Act, $39 billion is dedicated to incentivizing investment in facilities and equipment for the fabrication, assembly, testing, advanced packaging, or research and development of domestic semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment.

CPO is responsible for the implementation of the semiconductor incentive program. CPO established the following four objectives to achieve by 2030:

- **Leading-Edge Logic:** The United States will have at least two new large-scale clusters of leading-edge logic fabrication facilities. These clusters, consisting of multiple, commercial-scale fabrication facilities in geographically compact areas, are expected to produce roughly 20 percent of the world's leading-edge semiconductor chips.
- **Advanced Packaging:** The United States will be home to multiple high-volume advanced packaging facilities.
- **Leading-Edge Memory:** U.S.-based fabrication facilities will produce high-volume leading-edge dynamic random-access memory (DRAM) chips, remaining economically competitive in the global market.
- **Current-Generation and Mature-Node Semiconductors:** The United States will increase its production of the current generation and mature-node chips critical to economic and national security.

To help achieve these objectives, CPO issued two notices of funding opportunities (NOFOs): the Commercial Fabrication Facilities NOFO and the Facilities for Semiconductor Materials and Manufacturing Equipment NOFO. The following sections describe the two NOFOs and the Secure Enclave national security initiative. As of January 31, 2025, CPO has awarded up to approximately $33.7 billion of direct funding for the implementation of the semiconductor incentive program (see table 1).

Table 1. CPO Awards (in millions)

Funding Type	Direct Funding	Loans
Incentive awards	$30,663	$5,500
Secure enclave	$3,000	–
Awards subtotal	**$33,663**	**$5,500**
Administrative expenses	$753	–
Unawarded	$4,584	–
Total	**$39,000**	**$5,500**

Source: CPO and NIST's Grants Management Information System (GMIS)

Commercial Fabrication Facilities NOFO

The Commercial Fabrication Facilities NOFO was initially released on February 28, 2023, and subsequently amended on June 26, 2023. This NOFO invites applications for the construction, expansion, or modernization of:

- commercial facilities for the front and back-end fabrication of leading-edge, current-generation, and mature-node semiconductors;
- commercial facilities for wafer manufacturing; and
- commercial facilities for materials used to manufacture semiconductors and semiconductor equipment, where the capital investment is $300 million or more.

Funding Amount and Instruments

For this NOFO, CPO allocated up to $38.2 billion for direct funding and up to $75 billion in direct loans or loan guarantees. CHIPS incentives will be provided through grants, cooperative agreements, other transaction agreements (OTAs), loans, and loan guarantees.

Application Process

The application process for this NOFO consists of the following phases (shown in figure 1):

- **Statement of Interest (SOI):** Prior to submitting a pre-application or full application, applicants are required to submit an SOI. CPO uses SOIs to gauge interest in the program, assess the types of projects and applicants, and estimate staffing for subsequent applications.
- **Pre-Application:** This phase allows CPO to provide a preliminary assessment of the likelihood of a potential full application receiving CHIPS incentives and to provide feedback to applicants. This phase is optional for all projects.
- **Full Application:** This phase allows CPO to conduct a thorough merit review to determine whether a project adequately addresses the evaluation criteria and supports CHIPS strategic goals. If an application is determined to be complete and eligible according to the NOFO requirements and passes the merit review, the Department prepares a preliminary memorandum of terms (PMT). PMTs are nonbinding[2] agreements that outline key terms for a potential CHIPS incentives award, including the amount and form of the award.
- **Due Diligence:** The primary goals of this phase are to:
    - conduct a targeted validation of material facts in the application affecting investment success;
    - identify key risks; and
    - decide the extent to which these risks can be mitigated.
- **Award:** During the award phase, CPO negotiates the final award documents with applicants and ensures completion of applicant registration in systems required to manage awards and disbursements. Funding is expected to be disbursed as milestones are met.

[2] "Nonbinding" means the parties are not legally obligated to carry out the agreement's terms.

Figure 1. Commercial Fabrication Facilities NOFO Application Process

Phases shown in **green** are in process or completed.

Source: CPO

Application Data

Figure 2 shows the number of applications received by CPO by the deadline of June 18, 2024.

Figure 2. Commercial Fabrication Facilities NOFO Application Data

Source: CPO application data

Award Status

As of January 31, 2025, CPO has made 19 awards for up to $30.7 billion in direct funding and $5.5 billion in loans; see table 2 for award amounts by company. CPO will distribute the funds based on each company's completion of project milestones.

Table 2. Commercial Fabrication Facilities NOFO Funding Agreements (in millions)

Company	Direct Funding	Loans	Total Federal Investment
Taiwan Semiconductor	$6,565	$5,000	$11,565
Intel	$7,865	$0	$7,865
Micron	$6,165	$0	$6,165
Samsung	$4,745	$0	$4,745
Texas Instruments	$1,610	$0	$1,610
Global Foundries	$1,587	$0	$1,587
SK hynix	$458	$500	$958
Amkor Technology	$407	$0	$407
GlobalWafers	$406	$0	$406
Hemlock Semiconductor	$325	$0	$325
Polar Semiconductor	$123	$0	$123
Infinera	$93	$0	$93
Entegris	$77	$0	$77

Company	Direct Funding	Loans	Total Federal Investment
Absolics	$75	$0	$75
HP	$53	$0	$53
BAE	$36	$0	$36
Corning	$32	$0	$32
Rocket Lab (SolAero)	$24	$0	$24
Edwards Vacuum	$18	$0	$18
Total	**$30,663**	**$5,500**	**$36,163**

Source: CPO and GMIS. Totals may not sum due to rounding.

Table 3 shows the project scope and technology for the 10 largest projects, by company and location.

Table 3. 10 Largest Projects (in millions)

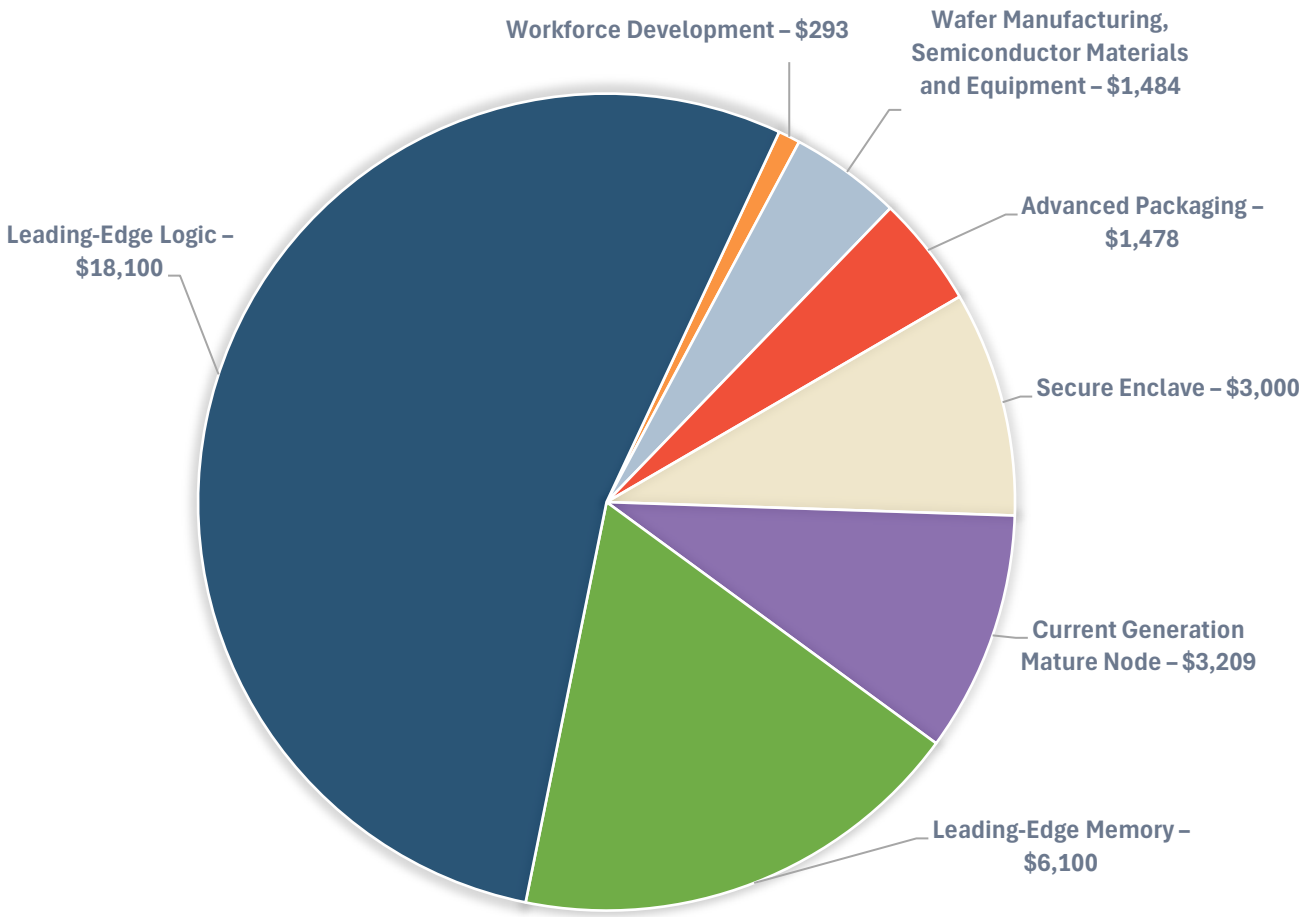
Company	Project Funds	Location	Technology	Project Scope
Taiwan Semiconductor	$6,500	Phoenix, AZ	Leading-Edge Logic	Construction of three fabrication facilities (fabs) focused on advanced chip design for machine learning/artificial intelligence
Micron	$4,600	Clay, NY	Leading-Edge Memory	Construction of two high-volume fabs focused on DRAM production
Samsung	$4,300	Taylor, Texas	Leading-Edge Logic	Construction of two foundries focused on production of advanced semiconductors supporting communications, automotives, defense, computing, and artificial intelligence and a research and development lab
Intel	$3,940	Chandler, AZ	Leading-Edge Logic	Construction of two new fabs and modernization of one existing fab, increasing manufacturing capacity of leading-edge chips
Intel	$1,860	Hillsboro, OR	Leading-Edge Logic	Modernization of existing fab to develop and produce advanced and future leading-edge chips
Intel	$1,500	New Albany, OH	Leading-Edge Logic	Construction of one greenfield fab to produce current and future leading-edge chips
Micron	$1,500	Boise, ID	Leading-Edge Memory	Construction of a high-volume fab focused on the DRAM production

Company	Project Funds	Location	Technology	Project Scope
Global Foundries	$1,450	Malta, NY	Current-Generation Mature-Node Advanced Packaging	Construction of a fab; expansion and modernization of an existing fab to provide advanced packaging and capacity expansion for the automotive industry
Texas Instruments	$900	Sherman, TX	Current-Generation Mature-Node	Construction of two fabs that are expected to produce analog and embedded processing chips
Texas Instruments	$700	Lehi, UT	Current-Generation Mature-Node	Construction of a fab to produce analog and embedded processing chips

Source: CPO

Figure 3 shows the distribution of funding by the primary project categories.

Figure 3. Funding by Category (in millions)



Source: CPO and GMIS

Next Steps

CPO accepted full applications until June 18, 2024. The review of applications is ongoing.

As of January 31, 2025, there are 15 nonbinding PMTs totaling up to approximately $1.9 billion in direct funding and $350 million in loans. The nonbinding PMTs are in the due diligence phase, during which material facts are validated, risks are addressed, and new information is reviewed that may affect the size, nature, or timing of the proposed awards.

Facilities for Semiconductor Materials and Manufacturing Equipment NOFO

The Facilities for Semiconductor Materials and Manufacturing Equipment NOFO was released on September 29, 2023. This NOFO seeks applications for projects for the construction, expansion, or modernization of commercial facilities for semiconductor materials and manufacturing equipment with capital investments of less than $300 million.

Funding Amount and Instruments

CPO reserved up to $500 million for direct funding for this NOFO. Funding incentives will be provided through grants, cooperative agreements, and OTAs.

Application Process

The application process for the Facilities for Semiconductor Materials and Manufacturing Equipment NOFO consists of the following phases (shown in figure 4):

- **Concept Plan:** Applicants are required to submit concept plans describing how their proposed project addresses core program priorities. Concept plans receive an initial review for eligibility, completeness, and responsiveness to the NOFO. Based on scoring from three independent reviewers, a written determination is made regarding whether the concept plan should or should not advance to the full application stage.
- **Full Application:** Full applications receive an initial review by the investment committee[3] for eligibility, completeness, and responsiveness to the NOFO. The investment committee makes a written determination based on the qualitative assessment, the program requirements, and the evaluation criteria regarding whether the application should advance to due diligence, be held for further consideration, or be denied.
- **Due Diligence:** Before entering into a final award for funding, the Department will conduct due diligence of the full application for national security risks, financial and commercial information, environmental impacts, and other issues, to inform a final decision on whether to make an award.
- **Award:** After due diligence, the investment committee may recommend an application to the selecting official, who must approve any applications for funding.

[3] The investment committee approves merit reviews for all applications, sizing and scoping, and proposed terms of PMTs.

Figure 4. Facilities for Semiconductor Materials and Manufacturing Equipment NOFO Application Process

Phases shown in **green** are in process or completed.

Source: CPO

Application Data

Figure 5 shows the number of concept plans, pre-applications, and full applications received by CPO by the deadline of July 1, 2024.

Figure 5. Facilities for Semiconductor Materials and Manufacturing Equipment NOFO Statistics

Source: CPO application data

Award Status

As of January 31, 2025, no awards have been made, and no funds have been committed or expended.

Next Steps

CPO accepted full applications until July 1, 2024. Completed applications are currently being reviewed in the full application phase.

Secure Enclave

The Secure Enclave is a national security initiative to create a secure supply of leading-edge semiconductors for the Department of Defense and the Intelligence Community. Congress allocated up to $3.5 billion of the $39 billion originally appropriated for the CHIPS Incentives Program to support the Secure Enclave. Specifically, the fiscal year (FY) 2024 Appropriations Act allocated $1.5 billion for FYs 2024 and 2025, and up to $500 million for FY 2026.

On September 16, 2024, Intel Corporation was awarded up to $3 billion in direct funding for the Secure Enclave. The award will be executed by the Department of Defense per an agreement with the Department of Commerce.

Due to the Secure Enclave funding requirement and high demand for CHIPS incentive funding, CPO announced on March 29, 2024, that it will not proceed with a NOFO for the construction, modernization, or expansion of semiconductor research and development facilities in the United States. CPO management said the Secure Enclave will affect other operations, including leading-edge facilities.

CHIPS Research and Development Office

Overview

Of the $50 billion provided to the Department by the CHIPS Act, $11 billion is designated for establishing a robust domestic semiconductor research and development ecosystem. CRDO manages this funding, overseeing a suite of programs aimed at enhancing the U.S. position in semiconductor research, development, and manufacturing.

CRDO is responsible for four integrated programs designed to foster innovation and competitiveness in the semiconductor industry:

- National Semiconductor Technology Center (NSTC) Program
- National Advanced Packaging Manufacturing Program (NAPMP)
- CHIPS Manufacturing USA Institute
- Metrology Program

The following sections describe the four integrated programs and CRDO-administered NOFOs for the Small Business Innovation Research Program and artificial intelligence (AI)-powered autonomous experimentation (AE) collaborations. As of January 31, 2025, CRDO has awarded almost $8.3 billion in funding for semiconductor research and development (see table 4).

Table 4. CRDO Awards by Program (in millions)

Program	Total Federal Investment
NSTC	$6,355
NAPMP	$1,400
CHIPS Manufacturing USA Institute	$285
Metrology	$252
Small Business Innovation Research	$5
Award subtotal	**$8,297**
Administrative expenses	$215
Unawarded	$2,488
Total	**$11,000**

Source: GMIS and Natcast OTAs; administrative expenses provided by CRDO

National Semiconductor Technology Center Program

The NSTC is a public-private consortium that includes participation from industry, universities, the Department of Commerce, the Department of Defense, the Department of Energy, and the National Science Foundation. Its goal is to advance semiconductor and microelectronics innovation with substantial financial and programmatic support from companies, universities, investors, and other government agencies, including those at the state and local levels. The membership program was launched on September 30, 2024.

Natcast, a nonprofit organization, was incorporated on October 19, 2023, to operate the NSTC. CRDO put together a committee of what NIST described as experienced industry leaders and executives with public and private sector experience to select the board of trustees to build and run Natcast. On November 9, 2023, the Department of Commerce announced it had reached an agreement with Natcast to operate the NSTC. During FY 2024, Natcast and its programs were funded by CHIPS Act appropriations using OTAs.[4] As of January 31, 2025, NIST awarded approximately $6.3 billion to Natcast to build the organization, operate the NSTC, identify key NSTC facilities, develop and scope research topics, issue calls for proposals and make awards, establish the Workforce Center of Excellence, and focus on priority programmatic areas.

Within the NSTC program, CRDO also established a pilot fellowship program and is working with the U.S. National Science Foundation (NSF) on the National Network for Microelectronics Education (NNME).

CHIPS Research and Development Pilot Fellowship Program

On July 9, 2024, CRDO issued an RFA to establish and manage a CHIPS Research and Development Pilot Fellowship Program. The program will fund fellowships for semiconductor industry entrepreneurs and provide resources needed to begin transitioning their semiconductor technology to commercialization.

- Funding Amount and Instruments

CRDO anticipates funding 10 fellowships, totaling $5 million, through a cooperative agreement.

- Application Selected

The RFA was noncompetitive. Activate Global Inc. was identified as the only eligible applicant.

- Next Steps

The 10 fellowships will be split into two cohorts, with the first cohort starting in 2025, and the second cohort starting in 2026. Applications for the first cohort were due on October 23, 2024. No funding has been expended as of January 31, 2025.

National Network for Microelectronics Education

On September 27, 2024, NSF and the Department of Commerce announced a $30 million funding opportunity to establish a Network Coordination Hub that will manage the NNME and lead its national strategy to train skilled workers needed in the U.S. semiconductor and microelectronics industry. NSF

[4] Under 15 U.S.C. 4659(a)(1), OTAs are agreements that are not considered contracts, grants, or cooperative agreements. OTAs are subject to "such terms as the Secretary considers appropriate."

will execute and manage the award process. The Department provided matching funds of $15 million to support this effort.

National Advanced Packaging Manufacturing Program

The NAPMP aims to expand U.S. capabilities in advanced packaging by forming a network of entities to create a robust domestic advanced packaging capacity. "Advanced packaging" refers to many chips with diverse functions assembled tightly together on a substrate[5] in two or three dimensions at extremely fine dimensions. This method achieves greater function, performance, and power efficiency compared with conventional packaged chips on a printed circuit board.

CRDO will work with a network of program participants to establish the National Advanced Packaging Piloting Facility (NAPPF), to enable the testing and integration of new approaches and processes in semiconductor advanced packaging. On January 16, 2025, CRDO awarded Natcast approximately $1.1 billion to operate the NAPPF.

NAPMP Materials and Substrates NOFO

The NAPMP Material and Substrates NOFO was released on February 28, 2024, to:

- accelerate domestic research and development and innovations in advanced packaging materials and substrates;
- translate domestic materials and substrate innovation into U.S. manufacturing;
- support the establishment of a robust, sustainable, domestic capacity for advanced packaging materials and substrate research and development, prototyping, commercialization, and manufacturing; and
- promote a skilled and diverse pipeline of workers for a sustainable domestic advanced packaging industry.

▶ Application Process

Applicants were required to submit a concept paper and full application that were assessed against four criteria: relevance to economic and national security, overall scientific and technical merit, project management, and transition and impact strategy.

▶ Application Data

Figure 6 shows the number of concept papers, invitations to complete a full application, and full applications received for the NAPMP Material and Substrates NOFO. Concept papers were due on April 12, 2024, and full applications were due on July 3, 2024.

[5] A substrate is the foundation or supporting base on or within which the elements of a semiconductor device are fabricated or attached.

Figure 6. NAPMP Materials and Substrates Application Data

Source: CRDO application data

▶ Award Status

On January 16, 2025, the Department announced three awards totaling $300 million for advanced substrates and material research (see table 5).

Table 5. NAPMP Materials and Substrates Awards (in millions)

Recipient	Amount
Absolics, Inc.	$100
Applied Materials, Inc.	$100
Arizona State University	$100
Total	**$300**

Source: CRDO announcement at Advanced Packaging Awards

NAPMP Advanced Packaging Research and Development NOFO

The NAPMP Advanced Packaging Research and Development NOFO was released on October 18, 2024, to seek proposals for activities that will accelerate domestic semiconductor advanced packaging through investments in the following five research and development areas:

- Equipment, tools, processes, and process integration
- Power delivery and thermal management
- Connector technology, including photonics and radio frequency
- Chiplets ecosystem
- Co-design/electronic design automation

▶ Funding Amount and Instruments

CRDO anticipates awarding up to approximately $1.5 billion in OTAs for multiple awards. Individual awards will be funded in amounts up to approximately $150 million, with a performance period of up to 5 years per award. CRDO is also reserving up to $50 million to support recipients under this NOFO pursuing prototyping activities. Prototypes will focus on application areas such as high-performance computing and low-power systems needed for AI.

▶ Application Process

Applicants were required to submit a concept paper that was assessed against five criteria: relevance to economic and national security; overall scientific and technical merit; project management,

resources, and budget; transition and impact strategy; and education and workforce development. CRDO will invite and accept full applications from selected applicants. Full applications will be assessed against the same five criteria.

- Application Data

Concept papers were due on December 20, 2024.

- Award Status

As of January 31, 2025, no awards have been made, and no funds have been committed or expended.

- Next Steps

CRDO is currently reviewing concept papers. Full applications will only be accepted from applicants who are invited to apply after concept papers are reviewed.

CHIPS Manufacturing USA Institute

Manufacturing USA is a national network of 17 institutes made up of manufacturing, government, and academic organizations. The network provides members with access to state-of-the-art facilities and equipment, promoting research, advancing new products to market, and supporting workforce training. NIST is seeking to establish a dedicated CHIPS Manufacturing USA Institute as part of this network.

CHIPS Manufacturing USA Institute Competition NOFO

On May 6, 2024, CRDO issued the CHIPS Manufacturing USA Institute Competition NOFO, soliciting proposals to establish and operate a CHIPS Manufacturing USA Institute. The institute will focus on semiconductor industry manufacturing challenges and will join the existing network of 17 institutes designed to increase the nation's manufacturing competitiveness and strengthen its research and development infrastructure.

The CHIPS Manufacturing USA Institute will manage a portfolio of institute-led projects and competitively funded member-led projects, including education and workforce development activities, basic and applied research, and technology demonstrations.

- Application Process

Applicants were required to submit a concept paper and full application that were assessed against five technical criteria: relevance to economic and national security; project management, resources, and budget; overall scientific and technical merit; transition and impact strategy; and education and workforce development.

- Application Data

Figure 7 shows the number of concept papers received and the invitations to complete a full application. Concept papers were due on June 20, 2024, and full applications were due on September 9, 2024.

Figure 7. CHIPS Manufacturing USA Application Data

Source: CRDO application data

- Award Status

On January 3, 2025, the Department announced it awarded the Semiconductor Research Corporation Manufacturing Consortium Corporation $285 million to establish and operate a Manufacturing USA institute known as SMART USA (Semiconductor Manufacturing and Advanced Research with Twins USA).

Metrology Program

According to NIST, the ability to measure semiconductors throughout the fabrication process is an essential part of enabling the high-yield and high-quality fabrication that is required for economic viability. Advances in the industry are driving ever more exacting requirements for materials purity, defect tolerances, materials properties, and in-line processes. Measurement capabilities must improve quickly for the CHIPS investments to yield full value. To support this effort to improve measurement capabilities, NIST will expand ongoing measurement science, or metrology, research programs intended to enable breakthroughs in measurement, standards, and process capabilities for the fabrication of next-generation semiconductors.

In addition to issuing the Measurement Science and Engineering (MSE) Research Grant Program NOFO, CRDO has funded 61 intramural projects valued at almost $250 million to develop new instruments, methods, data analysis, and models and simulations.

Measurement Science and Engineering Research Grant Program NOFO

The MSE Research Grant Program offered financial assistance within multiple NIST grant programs, including CHIPS. Financial support may be provided for conferences, workshops, or other technical research meetings that are relevant to the CRDO mission. Financial support may also be provided for programs that focus on conducting the metrology that is critical to the development of new materials, packaging, and production methods for semiconductors.

- Funding Amount and Instruments

CRDO anticipates funding individual projects in the range of $5,000 to $250,000 per year, with performance periods of up to 5 years. Grants and cooperative agreements will be used to issue the awards.

- Application Process

Applications are evaluated based on rationality, technical merit, staff and institutional capability to perform the work, and reasonableness of the budget compared to the proposed work.

▶ Application Data

CRDO received 13 applications as of September 30, 2024.

▶ Award Status

As of January 31, 2025, there have been eight awards, totaling $1.1 million (see table 6).

Table 6. Metrology MSE Cooperative Agreements

Recipient	Amount
The Regents of the University of California, Santa Barbara	$108,140
Michigan State University	$150,000
Theiss Research	$148,945
Theiss Research	$110,940
North Carolina State University	$199,558
Theiss Research	$122,360
California Institute of Technology	$147,275
University of Maryland	$160,000
Total	**$1,147,218**

Source: GMIS

▶ Next Steps

CRDO is accepting proposals on a rolling basis.

Small Business Innovation Research Program

On April 16, 2024, CRDO issued the SBIR NOFO to seek applications from eligible small businesses that want to explore the technical merit or feasibility of an innovative idea or technology with the aim of developing a viable product or service for the commercial microelectronics marketplace.

▶ Funding Amount and Instruments

CRDO anticipated funding approximately 24 awards in two phases. For Phase I, individual awards may be up to $283,500, with up to an additional $6,500 for technical and business assistance. Phase II awards may be up to $1.9 million, with up to an additional $50,000 for technical and business assistance. Cooperative agreements were used to issue the awards.

▶ Application Process

All applications were evaluated and judged on a competitive basis. Applications were initially screened to determine eligibility, completeness, and responsiveness. Applications passing the initial screening are then evaluated via a merit review process. Final selection decisions were made by the selecting official, the director of the CHIPS Metrology Program, or designee.

▶ Application Data

CRDO received 172 applications by the deadline of June 14, 2024.

▶ Award Status

On September 19, 2024, CRDO announced 17 awards to small businesses totaling more than $4.8 million (see table 7).

Table 7. Metrology SBIR Cooperative Agreements

Recipient	Amount
HighRI Optics, Inc.	$283,009
Recon RF	$286,787
Direct Electron LP	$289,292
Photon Spot, Inc.	$283,393
Sigray, Inc.	$289,703
PrimeNano Inc.	$259,848
Photothermal Spectroscopy Corporation	$283,489
Octave Photonics	$290,000
Tech-X Corporation	$289,992
Vapor Cell Technologies	$257,367
Virtual EM, Inc.	$277,930
The Provenance Chain Network	$283,427
Tiptek, LLC	$289,999
Exigent Solutions	$289,965
Laser Thermal Analysis	$289,830
Hummingbird Scientific	$283,500
Steam Instruments, Inc.	$289,529
Total	**$4,817,060**

Source: CRDO announcement at Award: CHIPS Metrology Program Small Business Innovation Research (SBIR)

▶ Next Steps

Award recipients are required to submit progress reports within 4 months of the award and a commercial viability and domestic production plan for any resulting intellectual property 7 months after the award. Projects that exhibit commercial application potential will be further developed in Phase II.

CHIPS AI-Powered AE for Rapid, Industry-Informed Sustainable Semiconductor Materials and Processes Competition NOFO

On October 30, 2024, CRDO issued the NOFO to:

- accelerate research into and delivery of targeted, industry-relevant, sustainable semiconductor materials and processes through the application of AI/AE;
- propagate models for incorporating sustainability metrics into semiconductor industry materials design and discovery, in addition to continued advancement in power, performance, area, cost, or other relevant technology metrics;
- expand the capabilities of emerging research institutions and other emerging research and development participants through cohesive, innovative teams of universities, industry, government labs, and other stakeholders; and
- build an exceptional workforce of university graduates and faculty with AI/AE research and development expertise.

The anticipated program outcomes are related to the NSTC, CHIPS Manufacturing USA Institute, and other CHIPS programs.

Funding Amount and Instruments

CRDO anticipates awarding funds totaling approximately $100 million through OTAs. Multiple awards ranging from approximately $20 to $40 million with a period of performance of up to 5 years will be awarded.

Application Data

Concept papers were due on January 13, 2025.

Next Steps

Full applications will be accepted from applicants who are invited to apply based on review of the concept papers.

OIG's CHIPS Oversight Efforts

Office of Audit and Evaluation

Our Office of Audit and Evaluation (OAE) supervises and conducts independent and objective audits and other reviews of Department programs and activities to ensure they operate economically, efficiently, and effectively. The CHIPS Act provided funding for OIG to provide oversight of CPO and CRDO funds that will be led by our OAE. Specifically, the CHIPS Act requires OIG to assess:

- Eligibility requirements for entities receiving funds
- Whether funds are used in accordance with requirements
- Whether entities have carried out commitments made to worker and community investment
- Whether entities receiving funds received sufficient guidance about a violation of the required agreement
- Whether the Secretary has provided timely notification to Congress about violations
- Whether the Secretary has sufficiently reviewed any entity engaging in listed exceptions

OIG's *Top Management and Performance Challenges Facing the Department of Commerce in Fiscal Year 2024* (OIG-24-002) highlighted key issues related to promoting growth in domestic semiconductor manufacturing and research, including:

- Hiring and retaining qualified staff in a competitive labor market
- Implementing adequate internal controls and oversight

Within OAE, the Semiconductor Division manages CHIPS oversight projects. In FY 2024, we issued the following product:

- Evaluation: *NIST Surpassed Hiring Goals for CHIPS But Did Not Develop a Comprehensive Workforce Plan,* Report No. OIG-24-023-I.

NIST reviewed a draft of this report and provided comments on March 26, 2025. We updated the report as appropriate.

Office of Investigations

Our Office of Investigations (OI) has created a strategic plan to supplement our audits and other reviews. OI's work helps the Department deter and detect fraud and hold grantees and subgrantees accountable for performance, which were identified as priority areas in OIG's *Top Management and Performance Challenges Facing the Department of Commerce in Fiscal Year 2024* and informed development of OI's strategic plan.

OI continues to implement the strategic plan's overarching goal with respect to CHIPS Act programs, supporting the Department's efforts to prevent and detect fraud and other criminal activity affecting these programs. OI also provides fraud awareness training to NIST personnel and other stakeholders.

REPORT

FRAUD & WASTE & ABUSE

HOTLINE

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